AMENDMENTS TO THE CLAIMS

1. (thrice amended) A receiver circuit arranged in a receiving unit of multiplex radio equipment, comprising:

an identifying circuit for identifying a demodulated signal at a predetermined identification level, said signal being obtained by demodulating a multilevel orthogonal modulated signal;

a clock regenerating circuit for regenerating a signal identification clock for said identifying circuit to supply said signal identification clock to said identifying circuit;

an equalizing circuit for subjecting said signal obtained by demodulating the multilevel orthogonal modulated signal to an equalizing process; and

a clock phase detecting unit for detecting a phase component of said signal identification clock based on errors between input and output signals of said equalizing circuit and then for supplying said phase component to said clock regenerating circuit;

wherein said clock phase detecting unit includes:

an error detecting unit for detecting a signal error between said input and output signals of said equalizing circuit; and

a clock phase calculating unit for detecting the phase component of said signal identification clock by calculating the detection outputs from said error detecting unit.

2. (thrice amended) A receiver circuit arranged in a receiving unit of multiplex radio equipment, comprising:

an identifying circuit for identifying a demodulated signal at a predetermined identification level, said signal being obtained by demodulating a multilevel orthogonal

modulated signal;

a clock regenerating circuit for regenerating a signal identification clock for said identifying circuit to supply said signal identification clock to said identifying circuit;

an equalizing circuit for subjecting said signal obtained by demodulating the multilevel orthogonal modulated signal to an equalizing process; and

a clock phase detecting unit for detecting a phase component of said signal identification clock based on input and output signals of said equalizing circuit and then for supplying said phase component to said clock regenerating circuit;

wherein said clock phase detecting unit comprising:

an error detecting unit for detecting a signal error between said input and output signals of said equalizing circuit;

a signal inclination detecting unit for detecting the inclination of said demodulated signal; and

a clock phase calculating unit for operating the phase component of said signal identification clock by calculating based on respective outputs from said error detecting unit and said signal inclination detecting unit.

8. (four times amended) A receiver circuit arranged in a receiving unit of multiplex radio equipment, comprising:

an identifying circuit for identifying a demodulated signal at a predetermined identification level, said signal being obtained by demodulating a multilevel orthogonal modulated signal;

a clock regenerating circuit for regenerating a signal identification clock for said

identifying circuit to supply said signal identification clock to said identifying circuit;

an equalizing circuit for subjecting said signal obtained by demodulating the multilevel orthogonal modulated signal to an equalizing process; and

a clock phase detecting unit for detecting a phase component of said signal identification clock based on input and output signals of said equalizing circuit and then for supplying said phase component to said clock regenerating circuit;

wherein said clock phase detecting unit comprises:

an error detecting unit for detecting an input signal to output signal error of said equalizing circuit;

a signal inclination detecting unit for detecting the inclination of said demodulated signal;

a clock phase calculating unit for detecting the phase component of said signal identification clock by calculating based on the respective outputs from said error detecting unit and said signal inclination detecting unit;

a specific signal judging unit for judging whether a specific signal exists; and

a gating unit for producing the phase component of said signal identification clock obtained by said clock phase calculating unit when said specific signal judging unit judges that said specific signal exists.

47. (amended) A receiver circuit arranged in a receiving unit of multiplex radio equipment, comprising:

an identifying circuit for identifying a demodulated signal at a predetermined identification level, said demodulated signal being obtained by demodulating a multilevel orthogonal modulated signal;

a clock regenerating circuit for regenerating a signal identification clock for said identifying circuit to supply said signal identification clock to said identifying circuit; and

a clock phase detecting section for detecting a phase component of said signal identification clock, based on clock-phase-detecting composite input information including [any] one of (i) a combination of the demodulated signal which is obtained by demodulating the multilevel orthogonal modulated signal and an equalized demodulated signal, and (ii) a combination of clock phase difference information to be supplied to said identifying circuit and signal error differential information obtained by said identifying circuit, and then supplying said phase component to said clock regenerating circuit,

said clock phase detecting section including

a difference detecting unit, responsive to the receipt of said composite input information, for detecting [any] one of (I) difference information between the demodulated signal and the equalized demodulated signal, and (II) a combination of the clock phase difference information and the signal error differential information, and

a clock phase calculating unit for calculating said phase component of said signal identification clock based on the output from said difference detecting unit.

48. (new) A receiver circuit arranged in a receiving unit of multiplex radio equipment, comprising:

an identifying circuit for identifying a demodulated signal at a predetermined identification level, said demodulated signal being obtained by demodulating a multilevel orthogonal modulated signal;

a clock regenerating circuit for regenerating a signal identification clock for said identifying circuit to supply said signal identification clock to said identifying circuit; and

a clock phase detecting section for detecting a phase component of said signal identification clock, based on clock-phase-detecting composite input information including a combination of the demodulated signal which is obtained by demodulating the multilevel orthogonal modulated signal and an equalized demodulated signal, and then supplying said phase component to said clock regenerating circuit,

said clock phase detecting section including

a difference detecting unit, responsive to the receipt of said composite input information, for detecting difference information between the demodulated signal and the equalized demodulated signal, and

a clock phase calculating unit for calculating said phase component of said signal identification clock based on the output from said difference detecting unit.

STATUS OF CLAIMS AND IDENTIFICATION OF SUPPORT

Claims 1-14, 47, and 48 are pending.

Claims 1, 2, 8, and 47 are amended herein.

Claim 48 is newly presented herein.

Support for the amendment to claims 1, 2, and 8 may be found in the original claims, and throughout the specification and figures. In particular, support for these amendments may be found in figures 1-6 showing a demodulated signal being input to an identifying circuit.

Support for the amendment to claim 47 may be found throughout the specification and figures. In particular, support for these amendments may be found in figures 1-6 showing a clock phase detecting unit receiving the two recited signals.

Support for new claim 48 may be found throughout the specification and figures. In particular, support for this new claim may be found in figures 1-3 showing a clock phase detecting unit receiving the two recited signals.